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PATENT

5298-02502/PM98019C

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**OFFICIAL**In re Application of:
Sethuraman et al.Group Art Unit: 2823
Examiner: Lee, H.

Serial No. 09/779,123

Atty. Dkt. No. 5298-02502

Filed: February 7, 2001

For: PLANARIZED SEMICONDUCTOR
INTERCONNECT TOPOGRAPHY AND
METHOD FOR POLISHING A METAL
LAYER TO FORM INTERCONNECTI hereby certify that this correspondence is being transmitted via
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Commissioner for Patents, P.O. Box 1450, Alexandria, VA
22313, on the date indicated below.July 19, 2004
Date

Kevin L. Daffer

AMENDMENT: RESPONSE TO OFFICE ACTION MAILED APRIL 28, 2004**Mail Stop Non-Fee Amendment**
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313

Dear Sir/ Madam:

This paper is submitted in response to the Office Action mailed April 28, 2004 to further highlight reasons why the application is in condition for allowance.

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks begin on page 2 of this paper.